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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,183	01/20/2004	Mie Matsuo	04173.0440	7695

22852 7590 12/19/2006

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EXAMINER	
SANDVIK, BENJAMIN P	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/19/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/759,183	MATSUO, MIE	
	Examiner	Art Unit	
	Ben P. Sandvik	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2 and 4-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2 and 4-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 9/22/2006 have been fully considered but they are not persuasive. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the combination of Mashino and Mikawa is argued by the applicant to lack suggestion or motivation to combine the references in the proposed manner. The semiconductor device of Mashino requires a semiconductor element formation layer 202 on which a transistor or other electronic element is realized (see Paragraph 82 of Mashino). Mikawa discloses, in essence, a semiconductor element formation layer on which transistors are formed in order to realize the transistor that comprises a memory device (see Figure 1 and Paragraph 43 of Mikawa). An essential component of these transistors is the source/drain which is necessary for operation; the diffusion layers of Mikawa provide the source and drains region to the device. One of ordinary skill will have the motivation to combine the Mashino and Mikawa references in order to provide source and drain regions to realize transistor circuitry; and will find in the Mikawa reference the specific factual and concrete evidence that forming diffusion patterns in a

semiconductor element formation layer will sufficiently provide the source and drain regions. It follows that since the through plug 217 of Mashino is formed to pass through and be surrounded by the semiconductor element formation layer 202, the combination of Mashino and Mikawa will result the through plug being formed to pass through and be surrounded by the diffusion layer pattern as in claim 1 of the present application.

Furthermore, the applicant argues that the combination of Mashino and Mikawa would render the invention unsatisfactory for its intended purpose because the conductor 217 would *necessarily be in contact* with the diffusion layer pattern and insulation film formed between the diffusion pattern. The examiner disagrees with this statement. The conductor 217 of Mashino is insulated for the semiconductor element formation layer 202 by the insulating layer 209, and further separated by the interconnection pattern 214. There is no suggestion in either Mashino or Mikawa that layers 209 and 214 would be omitted in the proposed combination. Hence, the conductor 217, which is not in contact with layer 202, would not be in contact with the diffusion layer pattern located in layer 202.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 4-9, 13-15 and 21-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mashino et al (U.S. PG Pub #20020190375), in view of Mikawa et al (U.S. PG Pub #20020115226).

With respect to **claims 2, 5, 8, 14, and 21**, Mashino teaches a semiconductor substrate (Fig. 10, 201), a semiconductor element formation layer (Fig. 10, 202) formed on the semiconductor substrate, and a through plug formed to be partly surrounded by the semiconductor element formation layer and to pass through the semiconductor element formation layer and the semiconductor substrate without being in contact with the formation layer (Fig. 10, 217) as set forth in claim 2; and furthermore teaches a pattern portion formed above the semiconductor element formation layer comprising copper and without being in contact with the through plug (Fig. 10, 205b and Paragraph 117), as set forth in claim 5; and a pattern portion formed above the semiconductor element formation layer comprising copper wherein the through plug is partly surrounded also by the pattern portion above the semiconductor element formation layer (Fig. 10, 205b and Paragraph 117), as set forth in claim 8; and that the through plug has a columnar electric conductor made of copper (Paragraph 98) and an insulation layer made of silicon oxide (Fig. 10, 209 and Paragraph 84), as set forth in claim 14.

Mashino does not teach that on the semiconductor element formation layer there is formed diffusion layer patterns or an insulation film formed between the plural diffusion layer patterns. Mikawa teaches a plurality of diffusion layer

patterns formed on a semiconductor substrate (Fig. 1, 11a), and an insulation film formed between the plural diffusion layer patterns on the semiconductor substrate (Fig. 1, 12), and furthermore that the insulation film is formed to isolate the plural diffusion layer patterns from one another, as set forth in claim 21. It would have been obvious to one of ordinary skill in the art at the time the invention was made provide the semiconductor element formation layer of Mashino with a diffusion layer pattern and insulation film as taught by Mikawa, and thereby forming the through plug to pass through and be partly surrounded by the diffusion layer pattern, in order to provide source and drain regions to realize memory cell transistors (Paragraph 43 of Mikawa).

With respect to **claims 7, 4, and 13**, Mashino teaches a semiconductor substrate (Fig. 10, 201), a semiconductor element formation layer (Fig. 10, 202) formed on the semiconductor substrate, a pattern portion formed above the semiconductor element formation layer using copper as a material thereof (Fig. 10, 205b and Paragraph 117), and a through plug formed to be partly surrounded by the semiconductor element formation layer and to pass through the semiconductor element formation layer and the semiconductor substrate without being in contact with the formation layer (Fig. 10, 217), as set forth in claim 7; and furthermore teaches that a pattern portion formed above the semiconductor element formation layer comprising copper and without being in contact with the through plug (Fig. 10, 205b and Paragraph 117), as set forth in claim 4; and that the through plug has a columnar electric conductor made of copper (Paragraph

98) and an insulation layer made of silicon oxide (Fig. 10, 209 and Paragraph 84), as set forth in claim 13.

Mashino does not teach that on the semiconductor element formation layer there is formed a plurality of diffusion layer patterns or an insulation film formed between the plural diffusion layer patterns to isolate the plural diffusion layer patterns from one another. Mikawa teaches a plurality of diffusion layer patterns formed on a semiconductor substrate (Fig. 1, 11a), and an insulation film formed between the plural diffusion layer patterns on the semiconductor substrate (Fig. 1, 12). It would have been obvious to one of ordinary skill in the art at the time the invention was made provide the semiconductor element formation layer of Mashino with a diffusion layer pattern and insulation film as taught by Mikawa, and thereby forming the through plug to pass through and be partly surrounded by the insulation film, in order to in order to provide source and drain regions to realize memory cell transistors (Paragraph 43 of Mikawa).

With respect to **claim 9, 6, and 15**, Mashino teaches a plurality of semiconductor chips (Fig. 11, 215), at least one of the plural semiconductor chips including: a semiconductor substrate (Fig. 10, 201), a semiconductor element formation layer (Fig. 10, 202) formed on the semiconductor substrate, a pattern portion formed above the semiconductor element formation layer using copper as a material thereof (Fig. 10, 205b and Paragraph 117), a through plug formed to be partly surrounded by the semiconductor element formation layer and to pass through the semiconductor element formation layer and the semiconductor

substrate without being in contact with the formation layer, the through plug being partly surrounded also by the pattern portion above the semiconductor element formation layer (Fig. 10, 217) and being insulated from the pattern portion (Fig. 10, 209), and a connecting member electrically connecting the through plugs of the at least one of the plural semiconductor chips to a semiconductor chip of the plural semiconductor chips other than the at least one of the plural semiconductor chips (Fig. 11, 210); and furthermore teaches a pattern portion formed above the semiconductor element formation layer comprising copper and without being in contact with the through plug (Fig. 10, 205b and Paragraph 117), as set forth in claim 6; and that the through plug has a columnar electric conductor made of copper (Paragraph 98) and an insulation layer made of silicon oxide (Fig. 10, 209 and Paragraph 84), as set forth in claim 15.

Mashino does not teach that on the semiconductor element formation layer there is formed a plurality of diffusion layer patterns or an insulation film formed between the plural diffusion layer patterns to isolate the plural diffusion layer patterns from one another. Mikawa teaches a plurality of diffusion layer patterns formed on a semiconductor substrate (Fig. 1, 11a), and an insulation film formed between the plural diffusion layer patterns on the semiconductor substrate (Fig. 1, 12). It would have been obvious to one of ordinary skill in the art at the time the invention was made provide the semiconductor element formation layer of Mashino with a diffusion layer pattern and insulation film as taught by Mikawa, and thereby forming the through plug to pass through and be

partly surrounded by the insulation film, in order to provide source and drain regions to realize memory cell transistors (Paragraph 43 of Mikawa).

With respect to **claims 22-24**, Mashino does not teach diffusion layer patterns are dummy diffusion layer patterns. Mikawa teaches diffusion layer patterns that are dummy diffusion layer patterns (Paragraph 50, Cell B). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the device of Mashino with a dummy diffusion pattern based on the teachings of Mikawa in order to create a dummy cell in the memory area.

Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mashino and Mikawa, further in view of Mayashita et al (U.S. PG Pub #2001045605).

With respect to **claim 10**, Mashino and Mikawa teach all of the limitations of claim 7, but do not teach that the plural diffusion layer patterns have a metal silicide layer. Mayashita teaches a diffusion layer pattern comprising a metal silicide layer (Paragraph 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose a metal silicide layer as taught by Mayashita on the diffusion layer patterns of Mashino and Mikawa in order to decrease the parasitic resistance of the device.

With respect to **claim 11**, Mashino and Mikawa teach all of the limitations of claim 2, but do not teach that the plural diffusion layer patterns have a metal silicide layer. Mayashita teaches a diffusion layer pattern comprising a metal silicide layer (Paragraph 4). It would have been obvious to one of ordinary skill in

the art at the time the invention was made to dispose a metal silicide layer as taught by Mayashita on the diffusion layer patterns of Mashino and Mikawa in order to decrease the parasitic resistance of the device.

With respect to **claim 12**, Mashino and Mikawa teach all of the limitations of claim 9, but do not teach that the plural diffusion layer patterns have a metal silicide layer. Mayashita teaches a diffusion layer pattern comprising a metal silicide layer (Paragraph 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to dispose a metal silicide layer as taught by Mayashita on the diffusion layer patterns of Mashino and Mikawa in order to decrease the parasitic resistance of the device.

Claims 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mashino and Mikawa, in view of Sakao (U.S. Patent #6166425).

With respect to **claims 16 and 19**, Mashino and Mikawa teach all of the limitations of claim 7, and furthermore Mashino teaches that a diameter of the through plug is 50 to 70 micrometers (Paragraph 95), but do not teach that a diameter of the through plug is larger than as interval between adjacent ones of the plural diffusion layer patterns. Sakao teaches a semiconductor device wherein the diffusion layers are spaced such that there is about 0.25 micrometers between diffusion layers (Col 15 Ln 29-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to create the combined product of Mashino and Mikawa having the distance

between the diffusion layers be smaller than a diameter of the plug of Mashino based on the diffusion layer pitch taught by Sakao in order to maintain a small device size.

With respect to **claim 17**, Mashino and Mikawa teach all of the limitations of claim 2, and furthermore Mashino teaches that a diameter of the through plug is 50 to 70 micrometers (Paragraph 95), but do not teach that a diameter of the through plug is larger than as interval between adjacent ones of the plural diffusion layer patterns. Sakao teaches a semiconductor device wherein the diffusion layers are spaced such that there is about 0.25 micrometers between diffusion layers (Col 15 Ln 29-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to create the combined product of Mashino and Mikawa having the distance between the diffusion layers be smaller than a diameter of the plug of Mashino based on the diffusion layer pitch taught by Sakao in order to maintain a small device size.

With respect to **claim 18**, Mashino and Mikawa teach all of the limitations of claim 9, and furthermore Mashino teaches that a diameter of the through plug is 50 to 70 micrometers (Paragraph 95), but do not teach that a diameter of the through plug is larger than as interval between adjacent ones of the plural diffusion layer patterns. Sakao teaches a semiconductor device wherein the diffusion layers are spaced such that there is about 0.25 micrometers between diffusion layers (Col 15 Ln 29-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to create the combined product

of Mashino and Mikawa having the distance between the diffusion layers be smaller than a diameter of the plug of Mashino based on the diffusion layer pitch taught by Sakao in order to maintain a small device size.

With respect to **claim 20**, Mashino and Mikawa teach all of the limitations of claim 9, and furthermore Mashino teaches that a diameter of the through plug is 50 to 70 micrometers (Paragraph 95), but do not teach that a diameter of the through plug is larger than as interval between adjacent ones of the plural diffusion layer patterns. Sakao teaches a semiconductor device wherein the diffusion layers are spaced such that there is about 0.25 micrometers between diffusion layers (Col 15 Ln 29-32). It would have been obvious to one of ordinary skill in the art at the time the invention was made to create the combined product of Mashino and Mikawa having the distance between the diffusion layers be smaller than a diameter of the plug of Mashino based on the diffusion layer pitch taught by Sakao in order to maintain a small device size.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ben P. Sandvik whose telephone number is (571) 272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

bps

LEONARDO ANDUJAR
PRIMARY EXAMINER